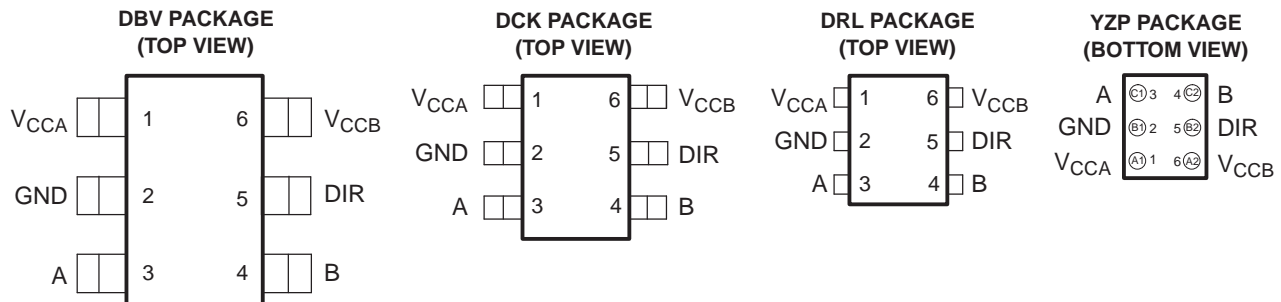


SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to V_{CCA}
- Low Power Consumption, 4- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Max Data Rates
 - 420 Mbps (3.3-V to 5-V Translation)
 - 210 Mbps (Translate to 3.3 V)
 - 140 Mbps (Translate to 2.5 V)
 - 75 Mbps (Translate to 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

The SN74LVC1T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess I_{CC} and I_{CCZ} .

The SN74LVC1T45 is designed so that the DIR input is powered by V_{CCA} .

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoFree is a trademark of Texas Instruments.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING ⁽³⁾ |
|----------------|--|--------------|-----------------------|---------------------------------|
| –40°C to 85°C | NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free) | Reel of 3000 | SN74LVC1T45YZPR | ___TA_ |
| | | Reel of 250 | SN74LVC1T45DBVT | CT1_ |
| | SOT (SOT-23) – DBV | Reel of 3000 | SN74LVC1T45DCKR | TA_ |
| | | Reel of 250 | SN74LVC1T45DCKT | |
| | SOT (SC-70) – DCK | Reel of 3000 | SN74LVC1T45DCKR | TA_ |
| | SOT (SOT-533) – DRL | Reel of 4000 | SN74LVC1T45DRLR | |

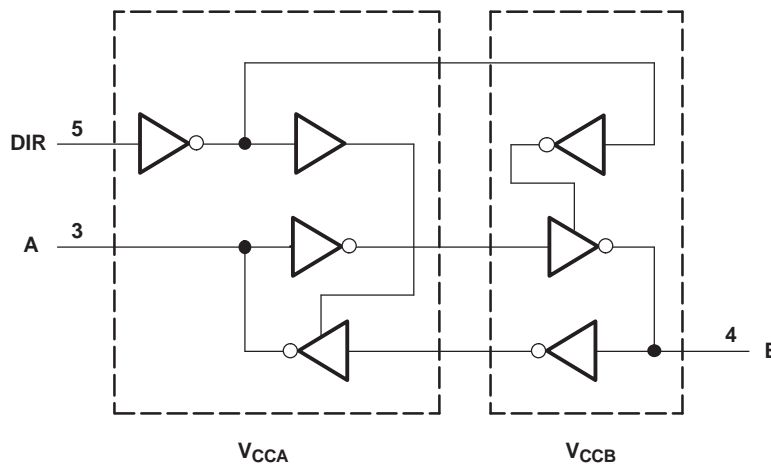
- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
- (3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site.
YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

FUNCTION TABLE⁽¹⁾

| INPUT DIR | OPERATION |
|-----------|-----------------|
| L | B data to A bus |
| H | A data to B bus |

- (1) Input circuits of the data I/Os always are active.

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT | |
|------------------------|---|-------------|------|-----------------|---|
| V_{CCA} V_{CCB} | Supply voltage range | –0.5 | 6.5 | V | |
| V_I | Input voltage range ⁽²⁾ | –0.5 | 6.5 | V | |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | –0.5 | 6.5 | V | |
| V_O | Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾ | A port | –0.5 | $V_{CCA} + 0.5$ | V |
| | | B port | –0.5 | $V_{CCB} + 0.5$ | |
| I_{IK} | Input clamp current | $V_I < 0$ | –50 | mA | |
| I_{OK} | Output clamp current | $V_O < 0$ | –50 | mA | |
| I_O | Continuous output current | | ±50 | mA | |
| | Continuous current through V_{CC} or GND | | ±100 | mA | |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DBV package | 165 | °C/W | |
| | | DCK package | 259 | | |
| | | DRL package | 142 | | |
| | | YZP package | 123 | | |
| T_{stg} | Storage temperature range | –65 | 150 | °C | |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾⁽²⁾⁽³⁾

| | | | V _{CCI} | V _{CCO} | MIN | MAX | UNIT |
|------------------|------------------------------------|---|------------------|------------------|-------------------------|-------------------------|------|
| V _{CCA} | Supply voltage | | | | 1.65 | 5.5 | V |
| V _{CCB} | | | | | 1.65 | 5.5 | |
| V _{IH} | High-level input voltage | Data inputs ⁽⁴⁾ | 1.65 V to 1.95 V | | V _{CCI} × 0.65 | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | V _{CCI} × 0.7 | | |
| V _{IL} | Low-level input voltage | Data inputs ⁽⁴⁾ | 1.65 V to 1.95 V | | | V _{CCI} × 0.35 | V |
| | | | 2.3 V to 2.7 V | | | 0.7 | |
| | | | 3 V to 3.6 V | | | 0.8 | |
| | | | 4.5 V to 5.5 V | | | V _{CCI} × 0.3 | |
| V _{IH} | High-level input voltage | DIR (referenced to V _{CCA}) ⁽⁵⁾ | 1.65 V to 1.95 V | | V _{CCA} × 0.65 | | V |
| | | | 2.3 V to 2.7 V | | 1.7 | | |
| | | | 3 V to 3.6 V | | 2 | | |
| | | | 4.5 V to 5.5 V | | V _{CCA} × 0.7 | | |
| V _{IL} | Low-level input voltage | DIR (referenced to V _{CCA}) ⁽⁵⁾ | 1.65 V to 1.95 V | | | V _{CCA} × 0.35 | V |
| | | | 2.3 V to 2.7 V | | | 0.7 | |
| | | | 3 V to 3.6 V | | | 0.8 | |
| | | | 4.5 V to 5.5 V | | | V _{CCA} × 0.3 | |
| V _I | Input voltage | | | | 0 | 5.5 | V |
| V _O | Output voltage | | | | 0 | V _{CCO} | V |
| I _{OH} | High-level output current | | 1.65 V to 1.95 V | | | –4 | mA |
| | | | 2.3 V to 2.7 V | | | –8 | |
| | | | 3 V to 3.6 V | | | –24 | |
| | | | 4.5 V to 5.5 V | | | –32 | |
| I _{OL} | Low-level output current | | 1.65 V to 1.95 V | | | 4 | mA |
| | | | 2.3 V to 2.7 V | | | 8 | |
| | | | 3 V to 3.6 V | | | 24 | |
| | | | 4.5 V to 5.5 V | | | 32 | |
| Δt/Δv | Input transition rise or fall rate | Data inputs | 1.65 V to 1.95 V | | | 20 | ns/V |
| | | | 2.3 V to 2.7 V | | | 20 | |
| | | | 3 V to 3.6 V | | | 10 | |
| | | | 4.5 V to 5.5 V | | | 5 | |
| | | Control inputs | 1.65 V to 5.5 V | | | 5 | |
| T _A | Operating free-air temperature | | | | –40 | 85 | °C |

(1) V_{CCI} is the V_{CC} associated with the input port.

(2) V_{CCO} is the V_{CC} associated with the output port.

(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V.

(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V.

Electrical Characteristics⁽¹⁾⁽²⁾

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | V _{CCA} | V _{CCB} | T _A = 25°C | | | –40°C to 85°C | | UNIT |
|--|-----------------|---|----------------------------------|------------------|---|-----|-----|---------------|---------------------------|------|
| | | | | | MIN | TYP | MAX | MIN | MAX | |
| V _{OH} | | I _{OH} = –100 μA I _{OH} = –4 mA I _{OH} = –8 mA I _{OH} = –24 mA I _{OH} = –32 mA | V _I = V _{IH} | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | V _{CCO} – 0.1 | V |
| | | | | 1.65 V | 1.65 V | | | 1.2 | | |
| | | | | 2.3 V | 2.3 V | | | 1.9 | | |
| | | | | 3 V | 3 V | | | 2.4 | | |
| | | | | 4.5 V | 4.5 V | | | 3.8 | | |
| V _{OL} | | I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 24 mA I _{OL} = 32 mA | V _I = V _{IL} | 1.65 V to 4.5 V | 1.65 V to 4.5 V | | | | 0.1 | V |
| | | | | 1.65 V | 1.65 V | | | 0.45 | | |
| | | | | 2.3 V | 2.3 V | | | 0.3 | | |
| | | | | 3 V | 3 V | | | 0.55 | | |
| | | | | 4.5 V | 4.5 V | | | 0.55 | | |
| I _I | DIR | V _I = V _{CCA} or GND | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | ±1 | ±2 | μA |
| I _{off} | A port | V _I or V _O = 0 to 5.5 V | 0 V | 0 to 5.5 V | | | | ±1 | ±2 | μA |
| | B port | | 0 to 5.5 V | 0 V | | | ±1 | ±2 | | |
| I _{OZ} | A or B port | V _O = V _{CCO} or GND | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | ±1 | ±2 | μA |
| I _{CCA} | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 3 | μA |
| | | | 5.5 V | 0 V | | | 2 | | | |
| | | | 0 V | 5.5 V | | | –2 | | | |
| I _{CCB} | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 3 | μA |
| | | | 5.5 V | 0 V | | | –2 | | | |
| | | | 0 V | 5.5 V | | | 2 | | | |
| I _{CCA} + I _{CCB} (see Table 1) | | V _I = V _{CCI} or GND, I _O = 0 | 1.65 V to 5.5 V | 1.65 V to 5.5 V | | | | | 4 | μA |
| ΔI _{CCA} | A port | A port at V _{CCA} – 0.6 V, DIR at V _{CCA} , B port = open | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | μA |
| | DIR | | | | DIR at V _{CCA} – 0.6 V, B port = open, A port at V _{CCA} or GND | | | | 50 | |
| ΔI _{CCB} | B port | B port at V _{CCB} – 0.6 V, DIR at GND, A port = open | 3 V to 5.5 V | 3 V to 5.5 V | | | | | 50 | μA |
| C _i | DIR | V _I = V _{CCA} or GND | 3.3 V | 3.3 V | | | | 2.5 | | pF |
| C _{io} | A or B port | V _O = V _{CCAB} or GND | 3.3 V | 3.3 V | | | | 6 | | pF |

 (1) V_{CCO} is the V_{CC} associated with the output port.

 (2) V_{CCI} is the V_{CC} associated with the input port.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------------|--------------|-------------|--|------|---|------|---|------|---|------|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 3 | 17.7 | 2.2 | 10.3 | 1.7 | 8.3 | 1.4 | 7.2 | ns |
| t_{PHL} | | | 2.8 | 14.3 | 2.2 | 8.5 | 1.8 | 7.1 | 1.7 | 7 | |
| t_{PLH} | B | A | 3 | 17.7 | 2.3 | 16 | 2.1 | 15.5 | 1.9 | 15.1 | ns |
| t_{PHL} | | | 2.8 | 14.3 | 2.1 | 12.9 | 2 | 12.6 | 1.8 | 12.2 | |
| t_{PHZ} | DIR | A | 5.2 | 19.4 | 4.8 | 18.5 | 4.7 | 18.4 | 5.1 | 17.1 | ns |
| t_{PLZ} | | | 2.3 | 10.5 | 2.1 | 10.5 | 2.4 | 10.7 | 3.1 | 10.9 | |
| t_{PHZ} | DIR | B | 7.4 | 21.9 | 4.9 | 11.5 | 4.6 | 10.3 | 2.8 | 8.2 | ns |
| t_{PLZ} | | | 4.2 | 16 | 3.7 | 9.2 | 3.3 | 8.4 | 2.4 | 6.4 | |
| $t_{PZH}^{(1)}$ | DIR | A | 33.7 | | 25.2 | | 23.9 | | 21.5 | | ns |
| $t_{PZL}^{(1)}$ | | | 36.2 | | 24.4 | | 22.9 | | 20.4 | | |
| $t_{PZH}^{(1)}$ | DIR | B | 28.2 | | 20.8 | | 19 | | 18.1 | | ns |
| $t_{PZL}^{(1)}$ | | | 33.7 | | 27 | | 25.5 | | 24.1 | | |

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------------|--------------|-------------|--|------|---|------|---|------|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 2.3 | 16 | 1.5 | 8.5 | 1.3 | 6.4 | 1.1 | 5.1 | ns |
| t_{PHL} | | | 2.1 | 12.9 | 1.4 | 7.5 | 1.3 | 5.4 | 0.9 | 4.6 | |
| t_{PLH} | B | A | 2.2 | 10.3 | 1.5 | 8.5 | 1.4 | 8 | 1 | 7.5 | ns |
| t_{PHL} | | | 2.2 | 8.5 | 1.4 | 7.5 | 1.3 | 7 | 0.9 | 6.2 | |
| t_{PHZ} | DIR | A | 3 | 8.1 | 3.1 | 8.1 | 2.8 | 8.1 | 3.2 | 8.1 | ns |
| t_{PLZ} | | | 1.3 | 5.9 | 1.3 | 5.9 | 1.3 | 5.9 | 1 | 5.8 | |
| t_{PHZ} | DIR | B | 6.5 | 23.7 | 4.1 | 11.4 | 3.9 | 10.2 | 2.4 | 7.1 | ns |
| t_{PLZ} | | | 3.9 | 18.9 | 3.2 | 9.6 | 2.8 | 8.4 | 1.8 | 5.3 | |
| $t_{PZH}^{(1)}$ | DIR | A | 29.2 | | 18.1 | | 16.4 | | 12.8 | | ns |
| $t_{PZL}^{(1)}$ | | | 32.2 | | 18.9 | | 17.2 | | 13.3 | | |
| $t_{PZH}^{(1)}$ | DIR | B | 21.9 | | 14.4 | | 12.3 | | 10.9 | | ns |
| $t_{PZL}^{(1)}$ | | | 21 | | 15.6 | | 13.5 | | 12.7 | | |

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------------|--------------|-------------|--|------|---|------|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 2.1 | 15.5 | 1.4 | 8 | 0.7 | 5.8 | 0.7 | 4.4 | ns |
| t_{PHL} | | | 2 | 12.6 | 1.3 | 7 | 0.8 | 5 | 0.7 | 4 | |
| t_{PLH} | B | A | 1.7 | 8.3 | 1.3 | 6.4 | 0.7 | 5.8 | 0.6 | 5.4 | ns |
| t_{PHL} | | | 1.8 | 7.1 | 1.3 | 5.4 | 0.8 | 5 | 0.7 | 4.5 | |
| t_{PHZ} | DIR | A | 2.9 | 7.3 | 3 | 7.3 | 2.8 | 7.3 | 3.4 | 7.3 | ns |
| t_{PLZ} | | | 1.8 | 5.6 | 1.6 | 5.6 | 2.2 | 5.7 | 2.2 | 5.7 | |
| t_{PHZ} | DIR | B | 5.4 | 20.5 | 3.9 | 10.1 | 2.9 | 8.8 | 2.4 | 6.8 | ns |
| t_{PLZ} | | | 3.3 | 14.5 | 2.9 | 7.8 | 2.4 | 7.1 | 1.7 | 4.9 | |
| $t_{PZH}^{(1)}$ | DIR | A | 22.8 | | 14.2 | | 12.9 | | 10.3 | | ns |
| $t_{PZL}^{(1)}$ | | | 27.6 | | 15.5 | | 13.8 | | 11.3 | | |
| $t_{PZH}^{(1)}$ | DIR | B | 21.1 | | 13.6 | | 11.5 | | 10.1 | | ns |
| $t_{PZL}^{(1)}$ | | | 19.9 | | 14.3 | | 12.3 | | 11.3 | | |

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Switching Characteristics

over recommended operating free-air temperature range, $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$ (see [Figure 1](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$ | | $V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$ | | $V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$ | | $V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$ | | UNIT |
|-----------------|--------------|-------------|--|------|---|-----|---|-----|---|-----|------|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | B | 1.9 | 15.1 | 1 | 7.5 | 0.6 | 5.4 | 0.5 | 3.9 | ns |
| t_{PHL} | | | 1.8 | 12.2 | 0.9 | 6.2 | 0.7 | 4.5 | 0.5 | 3.5 | |
| t_{PLH} | B | A | 1.4 | 7.2 | 1 | 5.1 | 0.7 | 4.4 | 0.5 | 3.9 | ns |
| t_{PHL} | | | 1.7 | 7 | 0.9 | 4.6 | 0.7 | 4 | 0.5 | 3.5 | |
| t_{PHZ} | DIR | A | 2.1 | 5.4 | 2.2 | 5.4 | 2.2 | 5.5 | 2.2 | 5.4 | ns |
| t_{PLZ} | | | 0.9 | 3.8 | 1 | 3.8 | 1 | 3.7 | 0.9 | 3.7 | |
| t_{PHZ} | DIR | B | 4.8 | 20.2 | 2.5 | 9.8 | 1 | 8.5 | 2.5 | 6.5 | ns |
| t_{PLZ} | | | 4.2 | 14.8 | 2.5 | 7.4 | 2.5 | 7 | 1.6 | 4.5 | |
| $t_{PZH}^{(1)}$ | DIR | A | 22 | | 12.5 | | 11.4 | | 8.4 | | ns |
| $t_{PZL}^{(1)}$ | | | 27.2 | | 14.4 | | 12.5 | | 10 | | |
| $t_{PZH}^{(1)}$ | DIR | B | 18.9 | | 11.3 | | 9.1 | | 7.6 | | ns |
| $t_{PZL}^{(1)}$ | | | 17.6 | | 11.6 | | 10 | | 8.6 | | |

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

Operating Characteristics

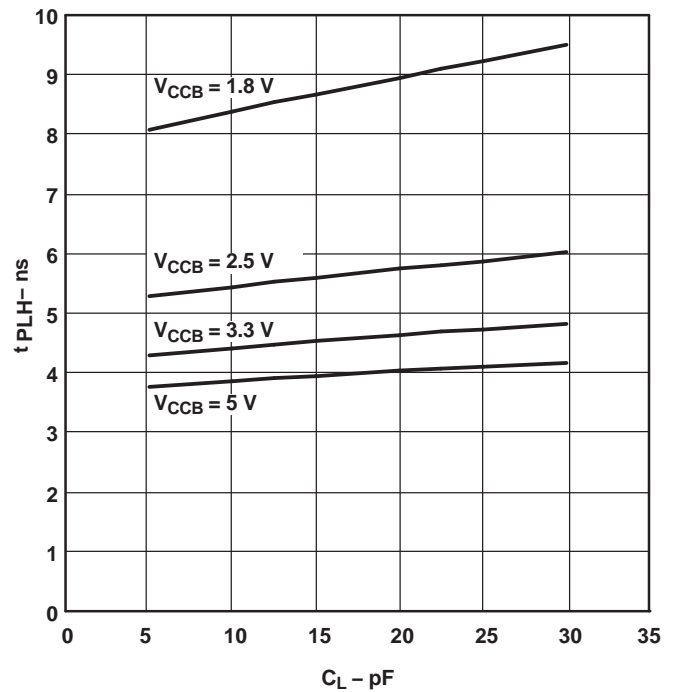
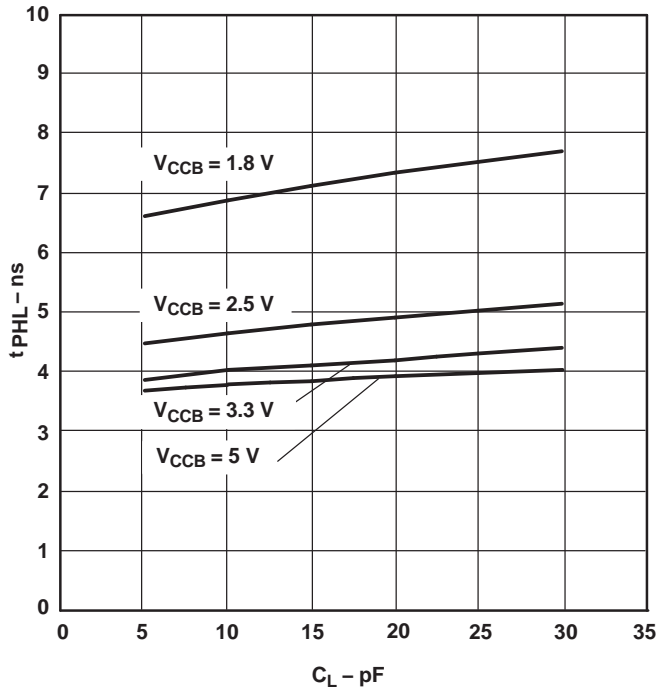
$T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | $V_{CCA} = V_{CCB} = 1.8 \text{ V}$ | $V_{CCA} = V_{CCB} = 2.5 \text{ V}$ | $V_{CCA} = V_{CCB} = 3.3 \text{ V}$ | $V_{CCA} = V_{CCB} = 5 \text{ V}$ | UNIT |
|-----------------|-----------------------------|-------------------------------------|-------------------------------------|-------------------------------------|-----------------------------------|------|
| | | TYP | TYP | TYP | TYP | |
| $C_{pdA}^{(1)}$ | A-port input, B-port output | 3 | 4 | 4 | 4 | pF |
| | B-port input, A-port output | | | | | |
| $C_{pdB}^{(1)}$ | A-port input, B-port output | 18 | 19 | 20 | 21 | pF |
| | B-port input, A-port output | | | | | |

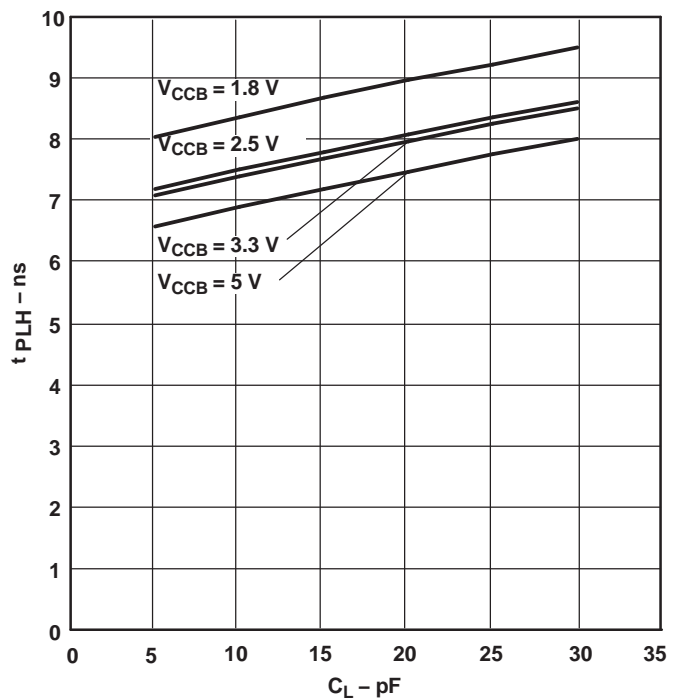
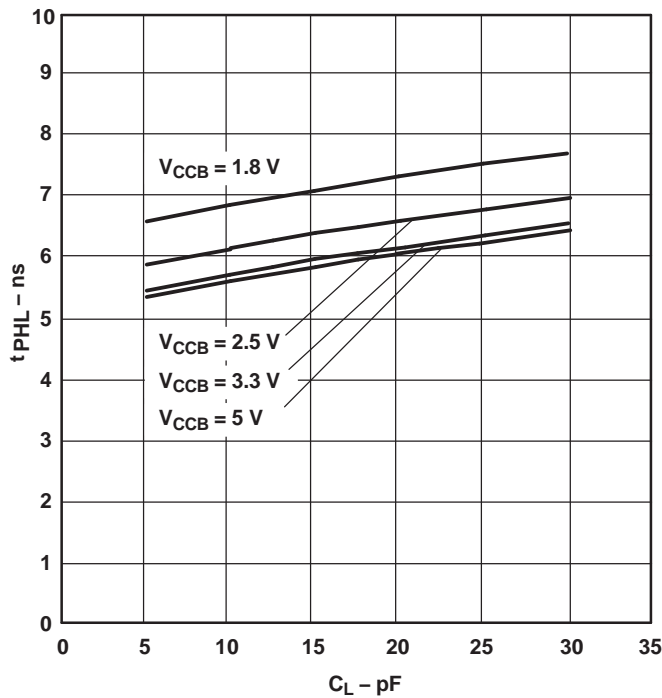
(1) Power dissipation capacitance per transceiver

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}, V_{CCA} = 1.8\text{ V}$

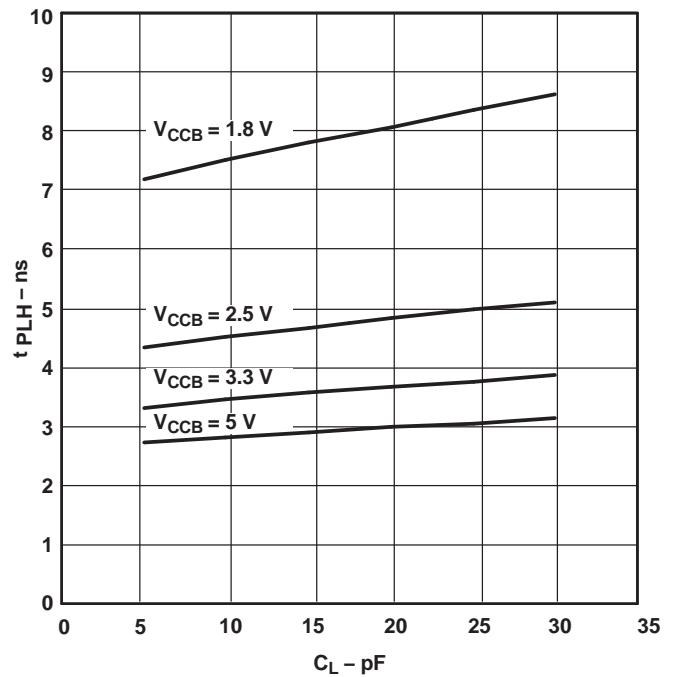
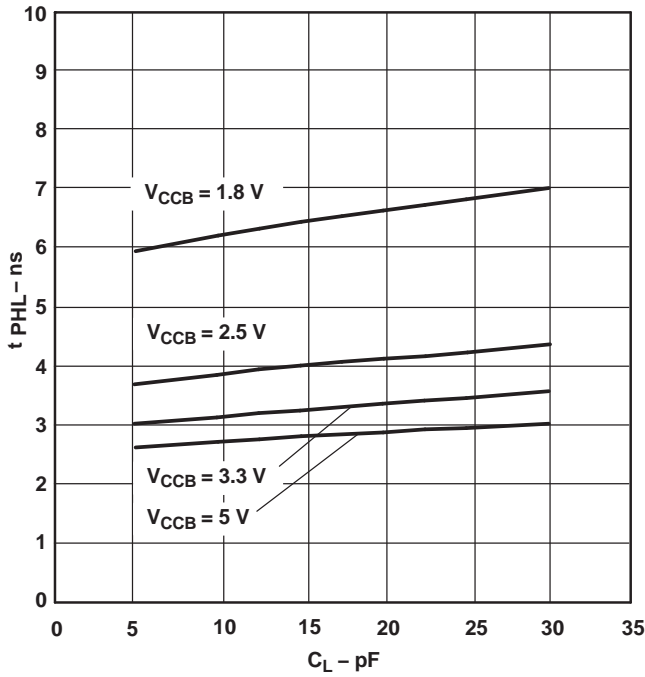


TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}, V_{CCA} = 1.8\text{ V}$

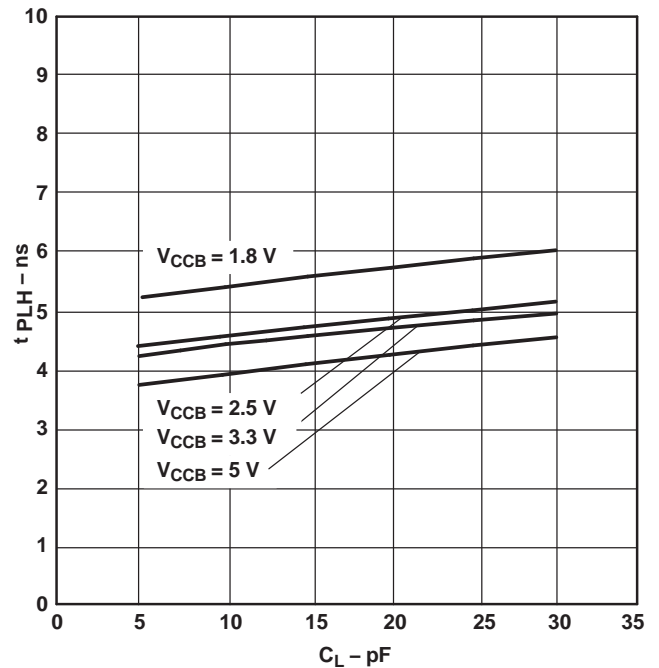
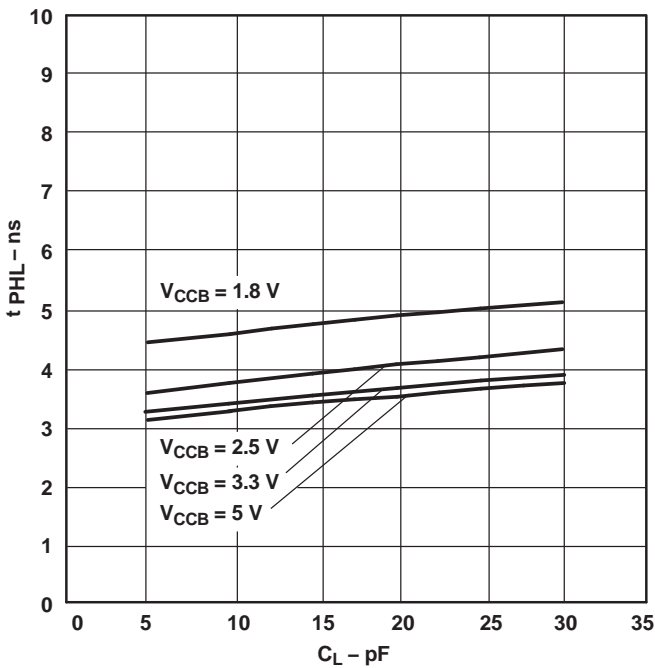


TYPICAL CHARACTERISTICS (continued)

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

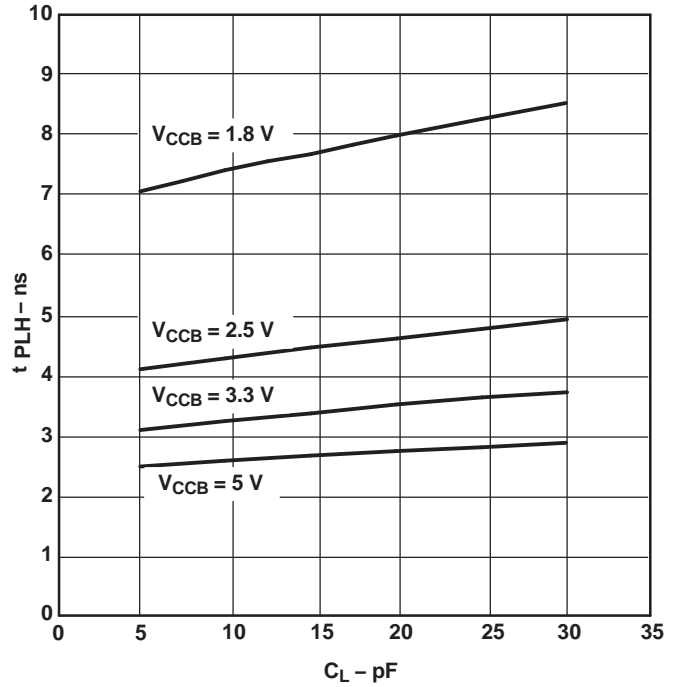
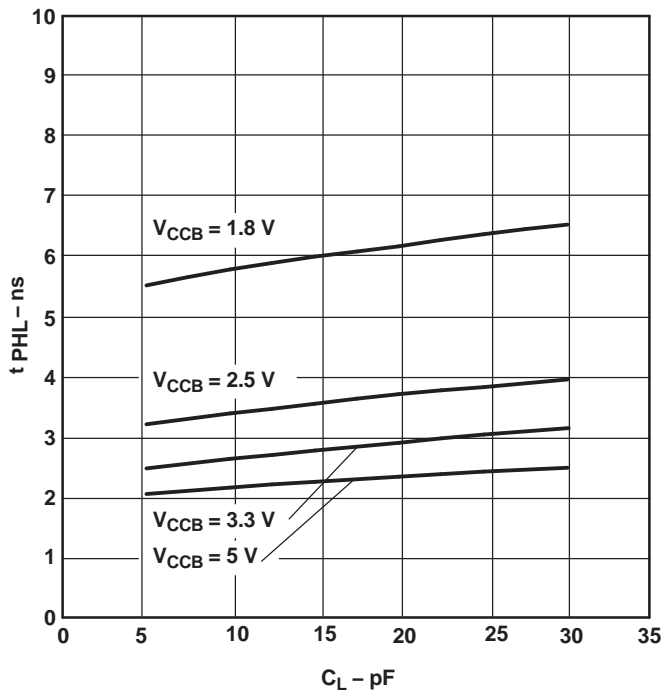


TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

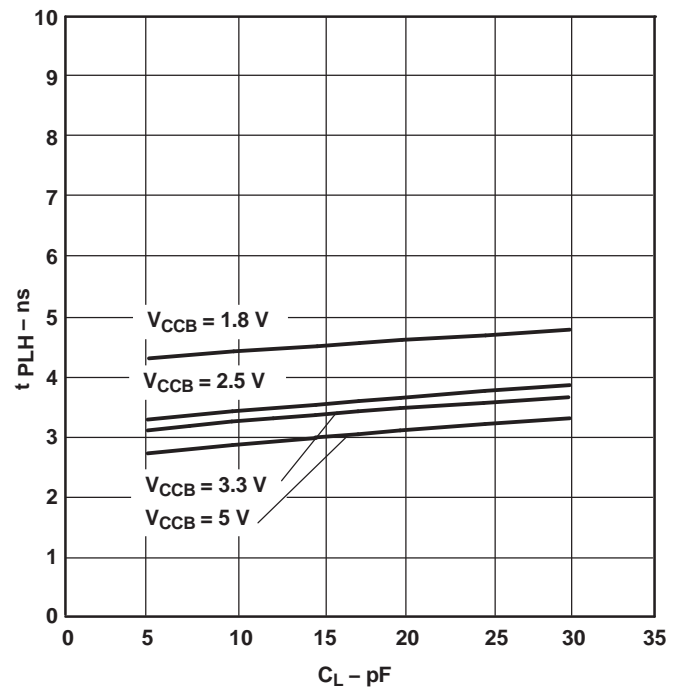
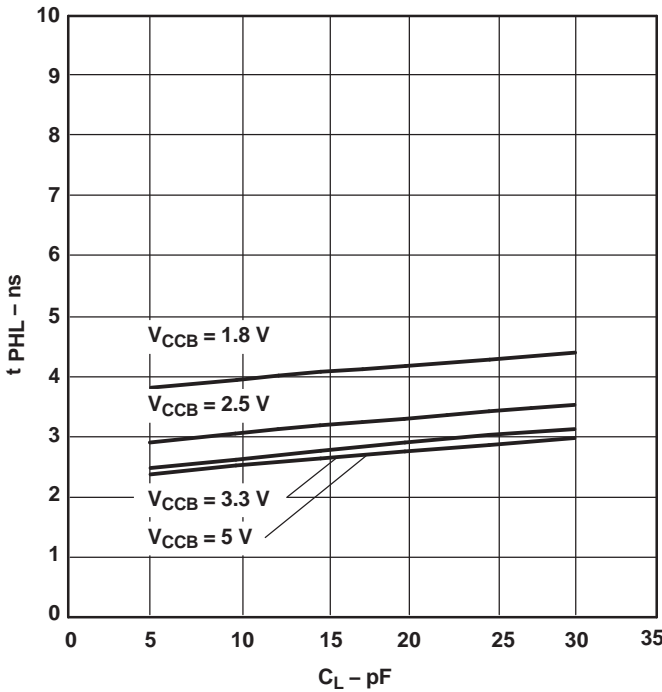


TYPICAL CHARACTERISTICS (continued)

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}, V_{CCA} = 3.3\text{ V}$

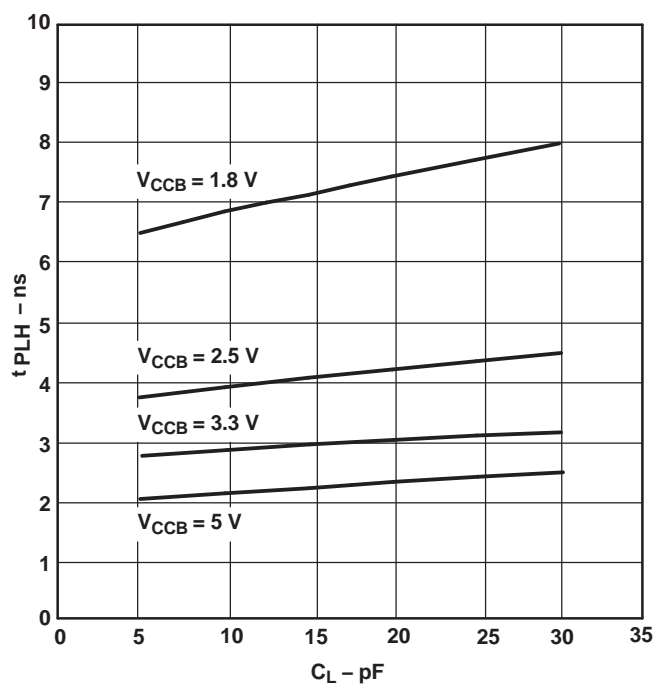
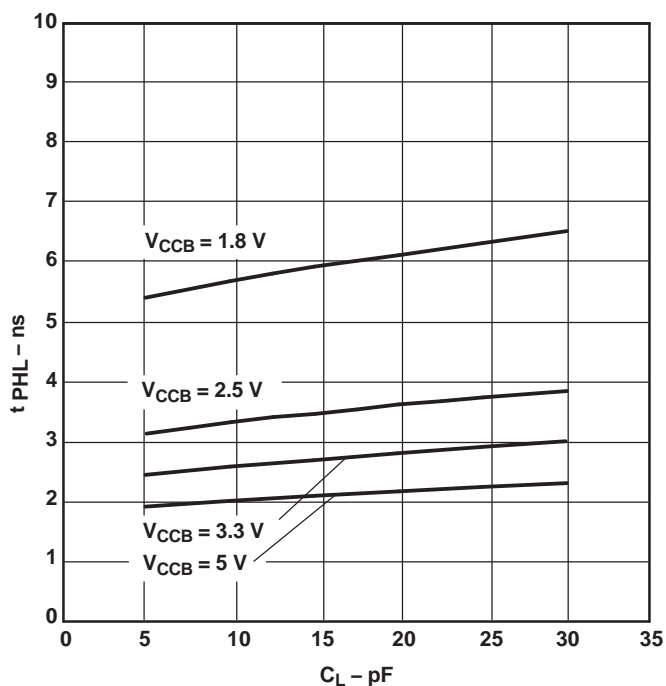


TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}, V_{CCA} = 3.3\text{ V}$

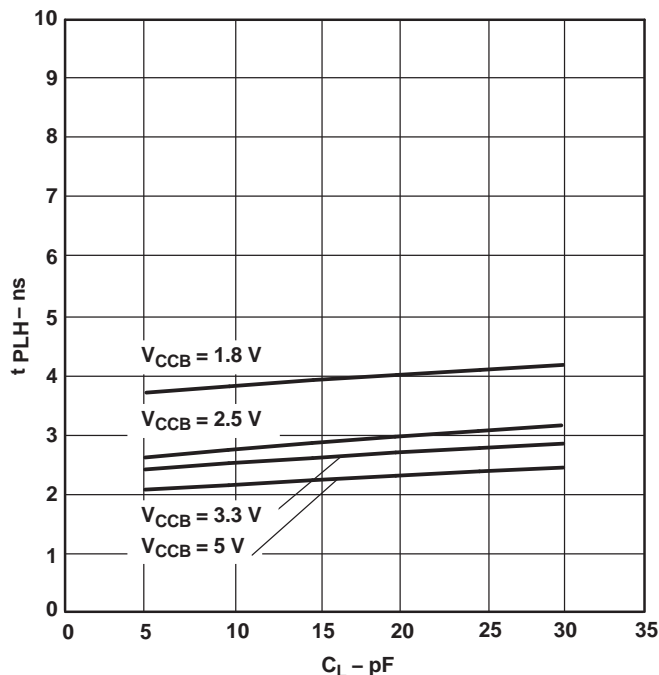
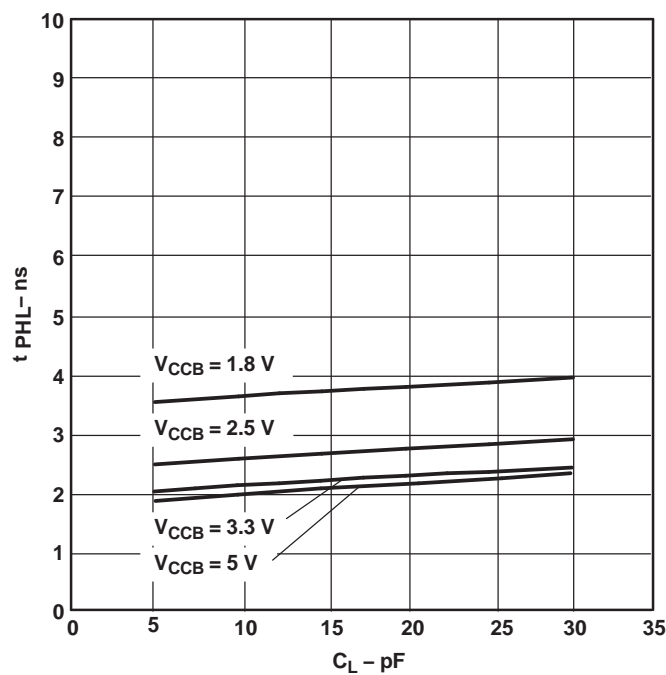


TYPICAL CHARACTERISTICS (continued)

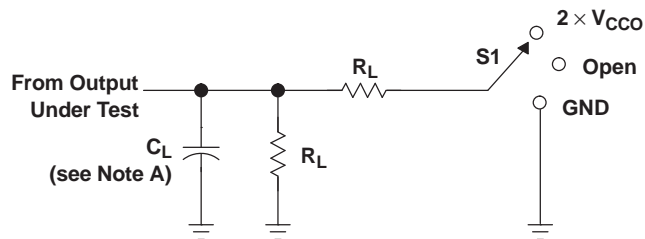
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$



TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 5\text{ V}$



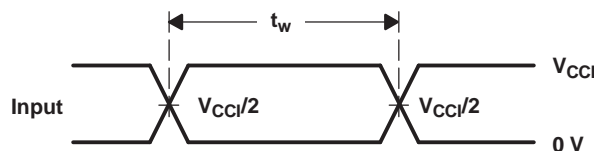
PARAMETER MEASUREMENT INFORMATION



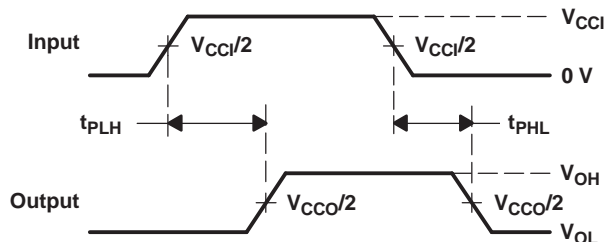
LOAD CIRCUIT

| TEST | S1 |
|-------------------|--------------------|
| t_{pd} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CCO}$ |
| t_{PHZ}/t_{PZH} | GND |

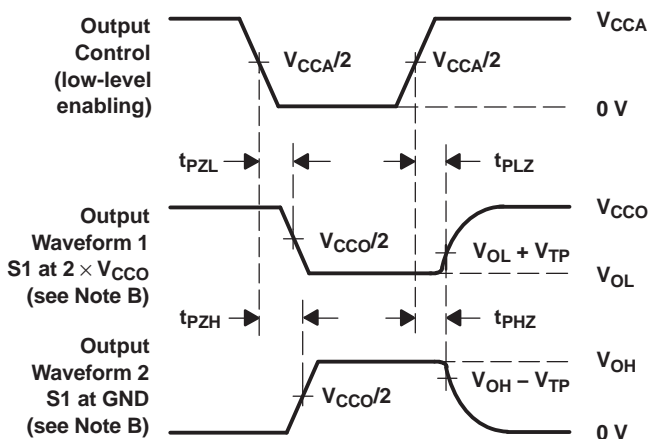
| V_{CCO} | C_L | R_L | V_{TP} |
|----------------------------------|-------|--------------|----------|
| $1.8\text{ V} \pm 0.15\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $2.5\text{ V} \pm 0.2\text{ V}$ | 15 pF | 2 k Ω | 0.15 V |
| $3.3\text{ V} \pm 0.3\text{ V}$ | 15 pF | 2 k Ω | 0.3 V |
| $5\text{ V} \pm 0.5\text{ V}$ | 15 pF | 2 k Ω | 0.3 V |



VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



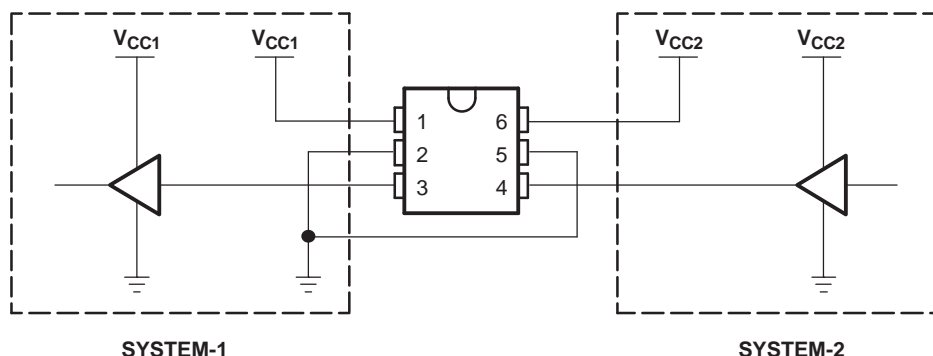
VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50\ \Omega$, $dv/dt \geq 1\text{ V/ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. V_{CCI} is the V_{CC} associated with the input port.
 - I. V_{CCO} is the V_{CC} associated with the output port.
 - J. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

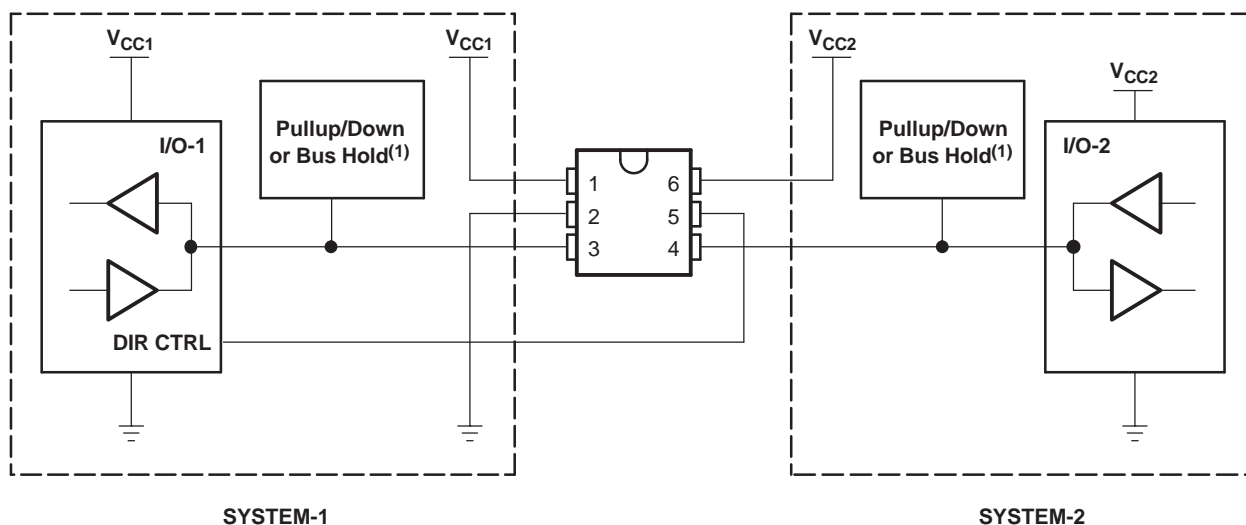
Figure 2 shows an example of the SN74LVC1T45 being used in a unidirectional logic level-shifting application.



| PIN | NAME | FUNCTION | DESCRIPTION |
|-----|------------------|------------------|--|
| 1 | V _{CCA} | V _{CC1} | SYSTEM-1 supply voltage (1.65 V to 5.5 V) |
| 2 | GND | GND | Device GND |
| 3 | A | OUT | Output level depends on V _{CC1} voltage. |
| 4 | B | IN | Input threshold value depends on V _{CC2} voltage. |
| 5 | DIR | DIR | GND (low level) determines B-port to A-port direction. |
| 6 | V _{CCB} | V _{CC2} | SYSTEM-2 supply voltage (1.65 V to 5.5 V) |

Figure 2. Unidirectional Logic Level-Shifting Application

Figure 3 shows the SN74LVC1T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

| STATE | DIR CTRL | I/O-1 | I/O-2 | DESCRIPTION |
|-------|----------|-------|-------|--|
| 1 | H | Out | In | SYSTEM-1 data to SYSTEM-2 |
| 2 | H | Hi-Z | Hi-Z | SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾ |
| 3 | L | Hi-Z | Hi-Z | DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾ |
| 4 | L | Out | In | SYSTEM-2 data to SYSTEM-1 |

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

Figure 3. Bidirectional Logic Level-Shifting Application

Enable Times

Calculate the enable times for the SN74LVC1T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC1T45DBVR | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DBVRE4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DBVRG4 | ACTIVE | SOT-23 | DBV | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DBVT | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DBVTE4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DBVTG4 | ACTIVE | SOT-23 | DBV | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (CT15 ~ CT1F ~ CT1R) | Samples |
| SN74LVC1T45DCKR | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DCKRE4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DCKRG4 | ACTIVE | SC70 | DCK | 6 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DCKT | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DCKTE4 | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DCKTG4 | ACTIVE | SC70 | DCK | 6 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA5 ~ TAF ~ TAR) | Samples |
| SN74LVC1T45DPKR | ACTIVE | USON | DPK | 6 | 5000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | TA7 | Samples |
| SN74LVC1T45DRLR | ACTIVE | SOT | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA7 ~ TAR) | Samples |
| SN74LVC1T45DRLRG4 | ACTIVE | SOT | DRL | 6 | 4000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | -40 to 85 | (TA7 ~ TAR) | Samples |
| SN74LVC1T45YZPR | ACTIVE | DSBGA | YZP | 6 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | (TA2 ~ TA7 ~ TAN) | Samples |

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN74LVC1T45 :

● Automotive: [SN74LVC1T45-Q1](#)

● Enhanced Product: [SN74LVC1T45-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1T45DBVR | SOT-23 | DBV | 6 | 3000 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 8.4 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DBVT | SOT-23 | DBV | 6 | 250 | 178.0 | 9.0 | 3.23 | 3.17 | 1.37 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DCKR | SC70 | DCK | 6 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 180.0 | 8.4 | 2.25 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.2 | 2.4 | 2.4 | 1.22 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DPKR | USON | DPK | 6 | 5000 | 180.0 | 9.5 | 1.75 | 1.75 | 0.7 | 4.0 | 8.0 | Q2 |
| SN74LVC1T45DRLR | SOT | DRL | 6 | 4000 | 180.0 | 8.4 | 1.98 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45DRLR | SOT | DRL | 6 | 4000 | 180.0 | 9.5 | 1.78 | 1.78 | 0.69 | 4.0 | 8.0 | Q3 |
| SN74LVC1T45YZPR | DSBGA | YZP | 6 | 3000 | 178.0 | 9.2 | 1.02 | 1.52 | 0.63 | 4.0 | 8.0 | Q1 |

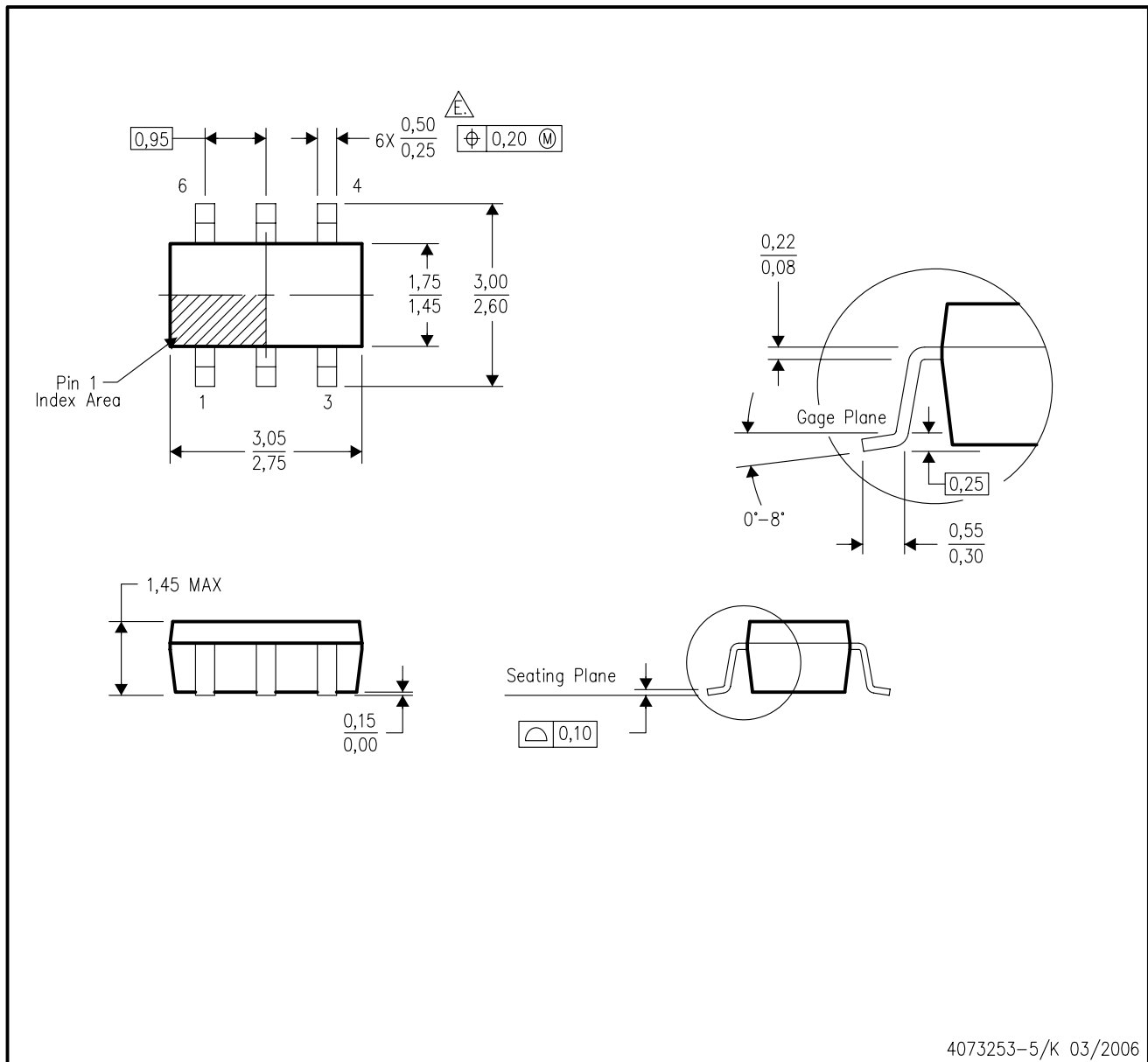
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1T45DBVR | SOT-23 | DBV | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1T45DBVR | SOT-23 | DBV | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1T45DBVT | SOT-23 | DBV | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1T45DBVT | SOT-23 | DBV | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1T45DCKR | SC70 | DCK | 6 | 3000 | 180.0 | 180.0 | 18.0 |
| SN74LVC1T45DCKR | SC70 | DCK | 6 | 3000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 202.0 | 201.0 | 28.0 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1T45DCKT | SC70 | DCK | 6 | 250 | 180.0 | 180.0 | 18.0 |
| SN74LVC1T45DPKR | USON | DPK | 6 | 5000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1T45DRLR | SOT | DRL | 6 | 4000 | 202.0 | 201.0 | 28.0 |
| SN74LVC1T45DRLR | SOT | DRL | 6 | 4000 | 180.0 | 180.0 | 30.0 |
| SN74LVC1T45YZPR | DSBGA | YZP | 6 | 3000 | 220.0 | 220.0 | 35.0 |

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
- $\triangle E$ Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

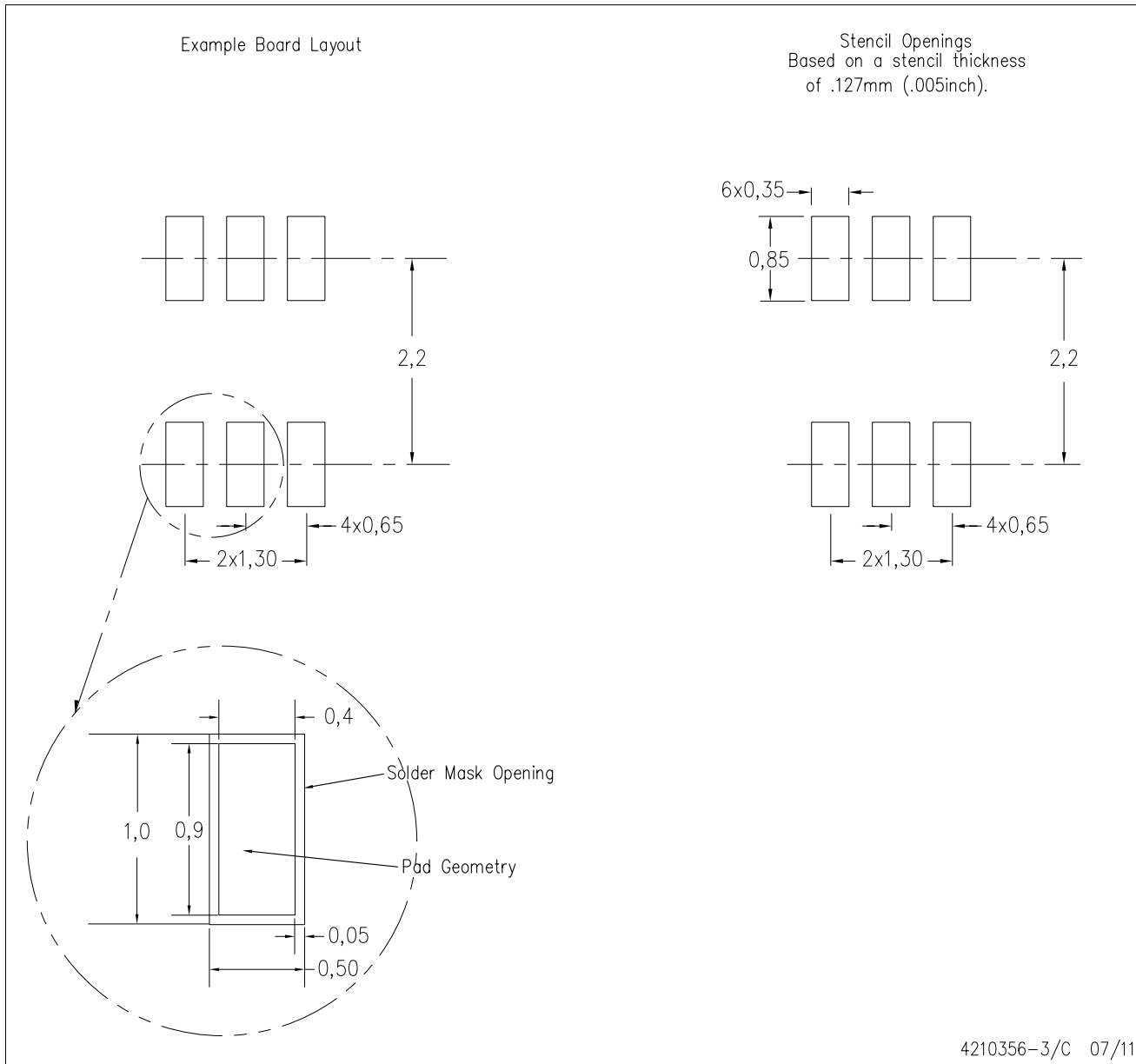
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DCK (R-PDSO-G6)

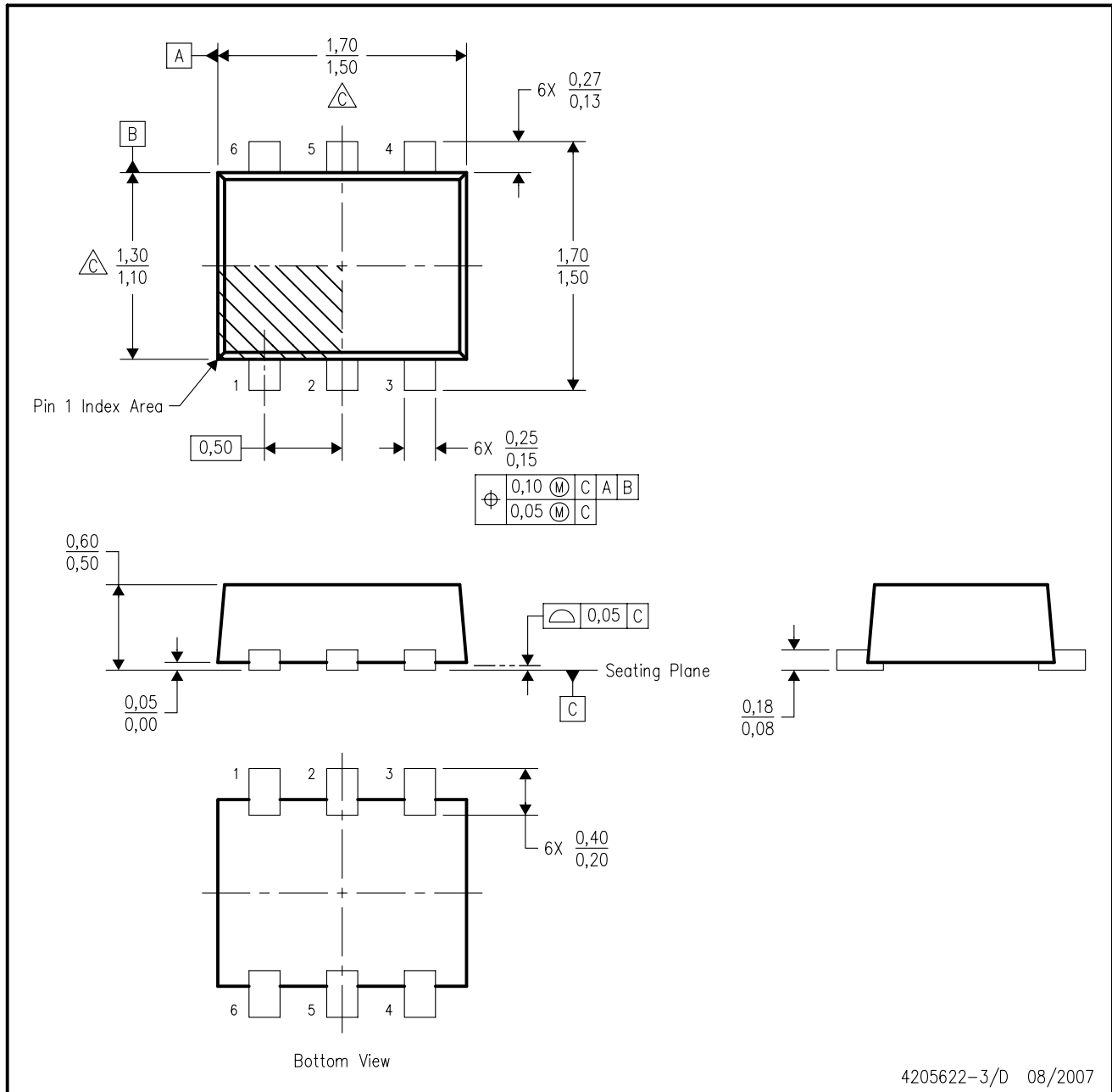
PLASTIC SMALL OUTLINE



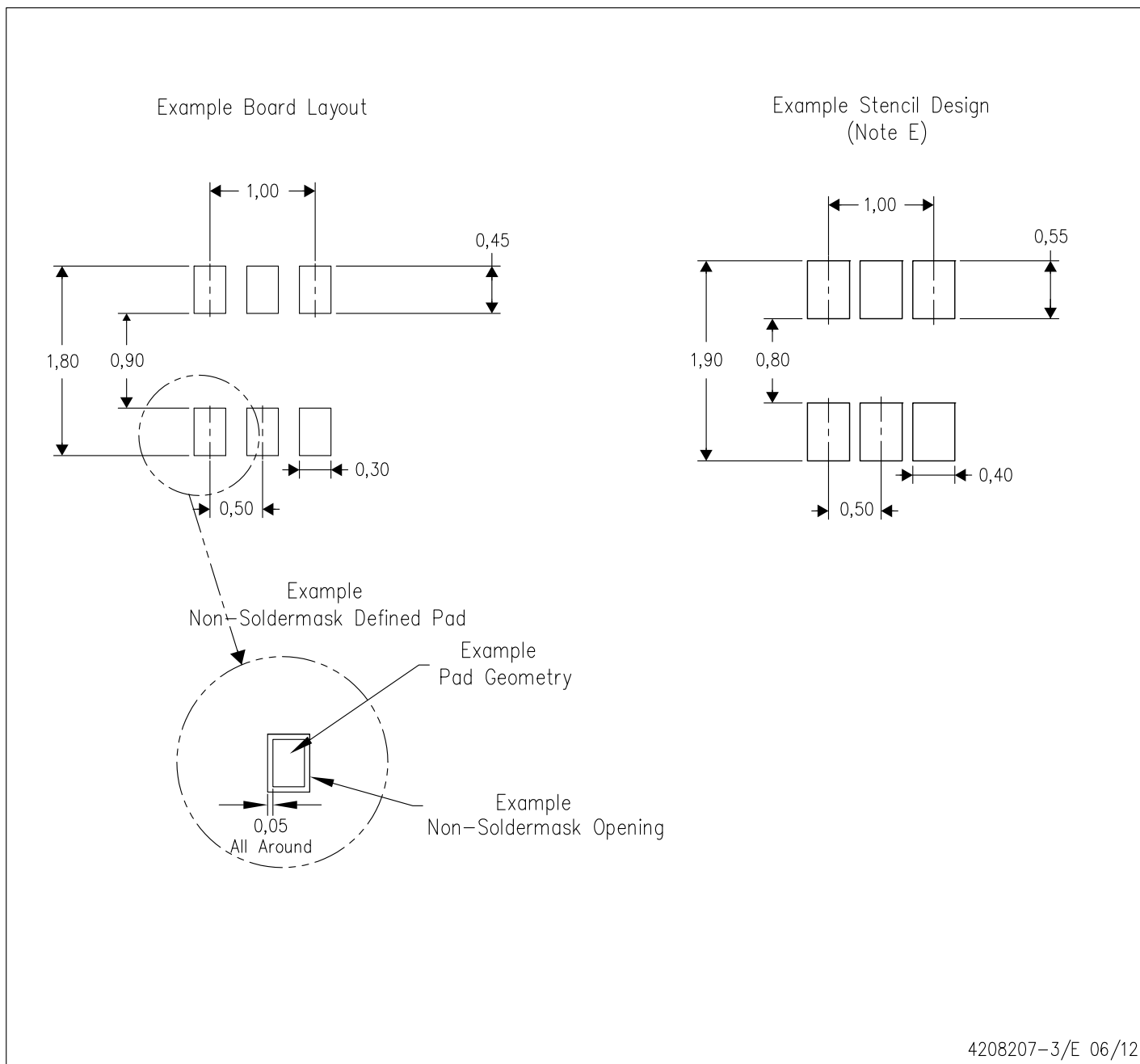
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DRL (R-PDSO-N6)

PLASTIC SMALL OUTLINE



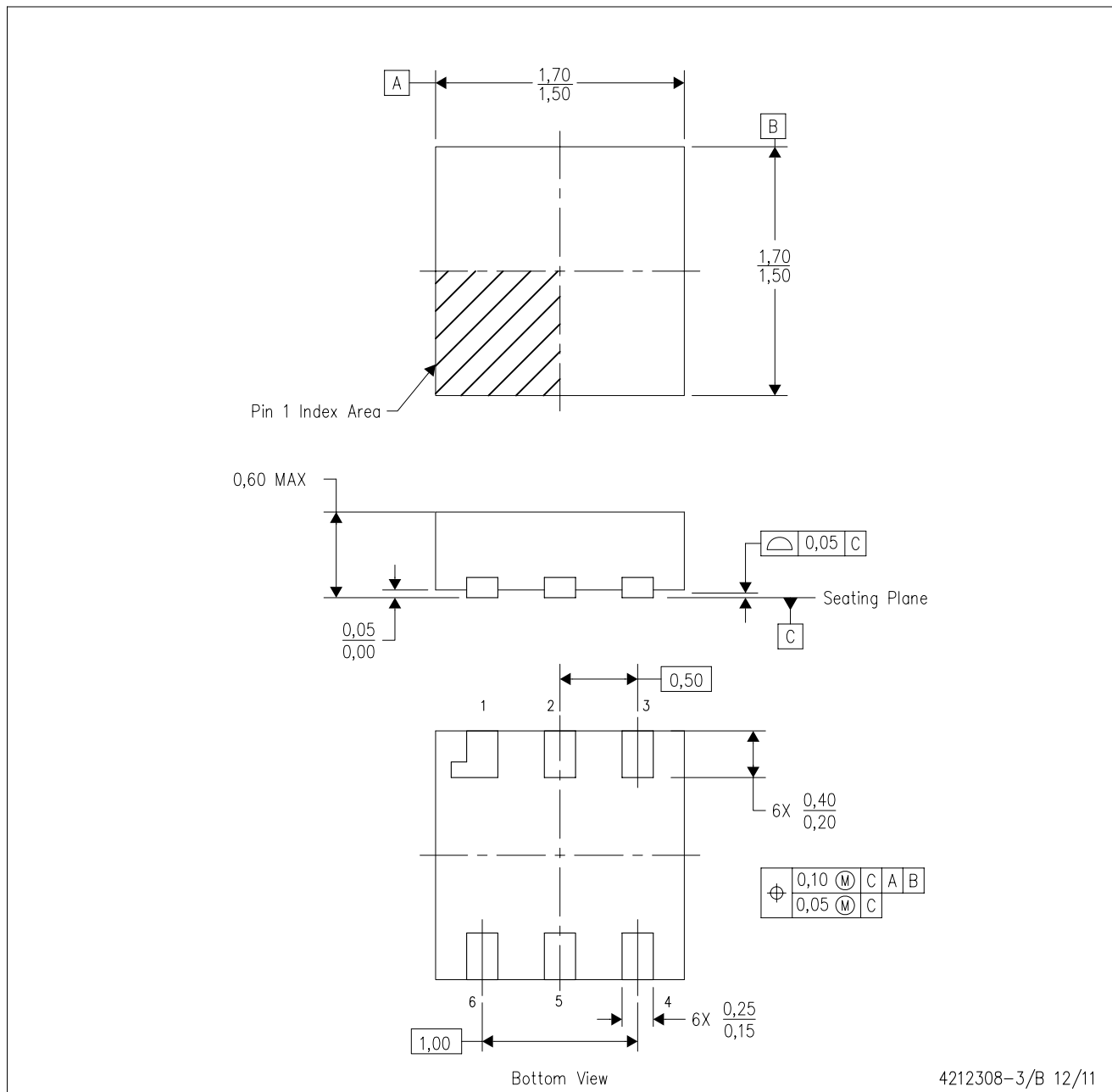
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash, interlead flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0,15 per end or side.
 - D. JEDEC package registration is pending.



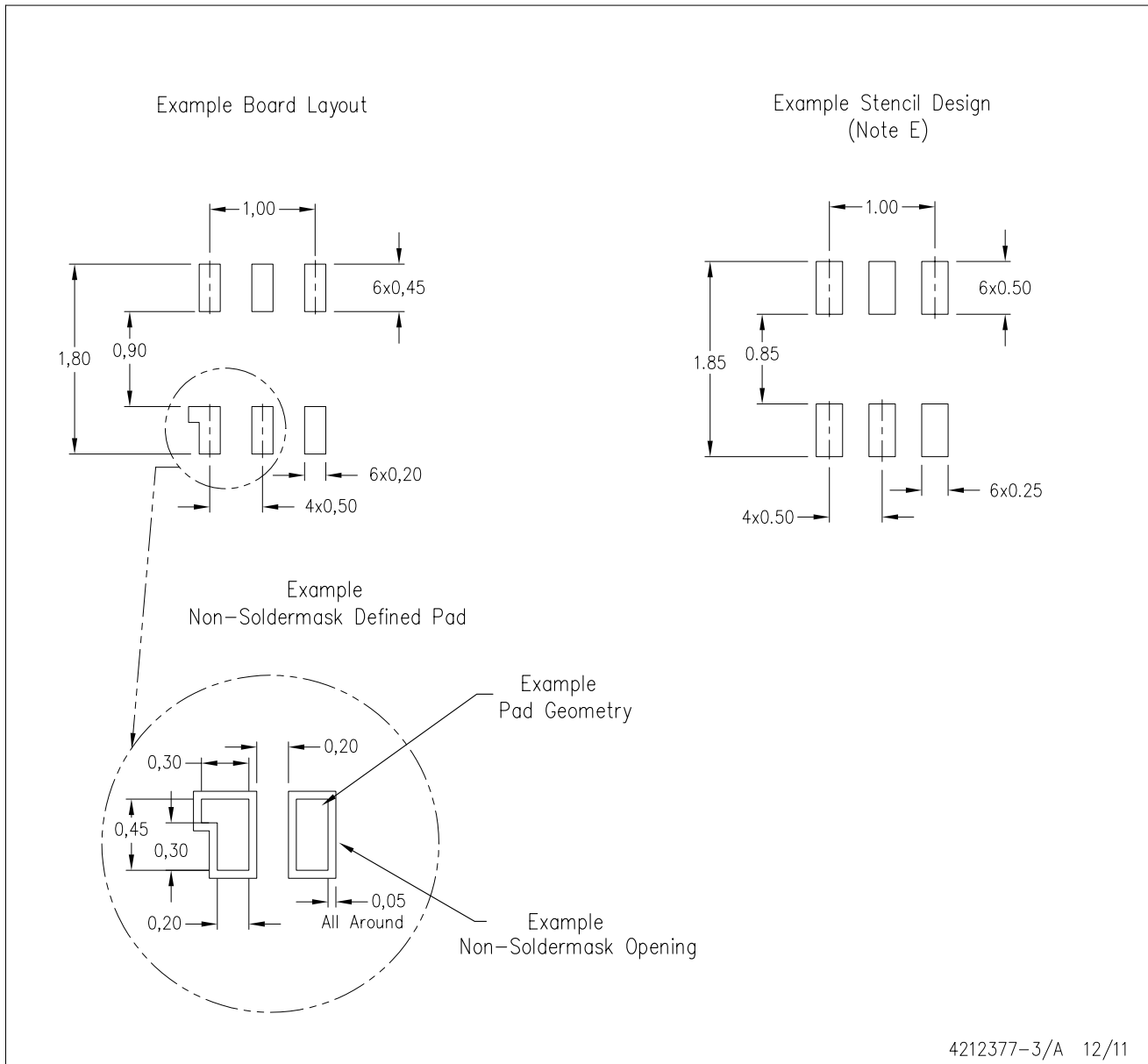
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

DPK (S-PUSON-N6)

PLASTIC SMALL OUTLINE NO-LEAD



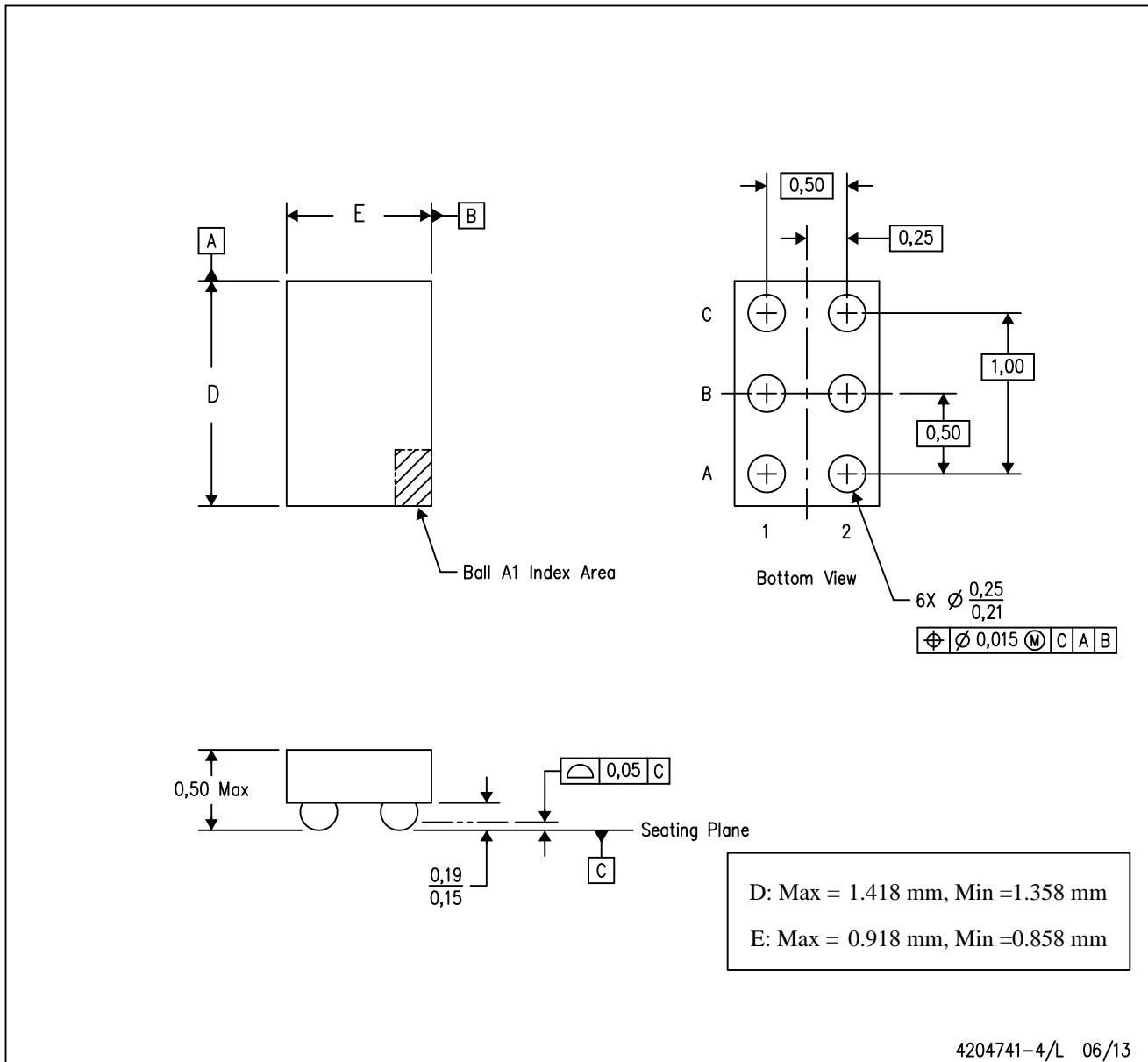
NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 B. This drawing is subject to change without notice.



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

YZP (R-XBGA-N6)

DIE-SIZE BALL GRID ARRAY



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 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

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